

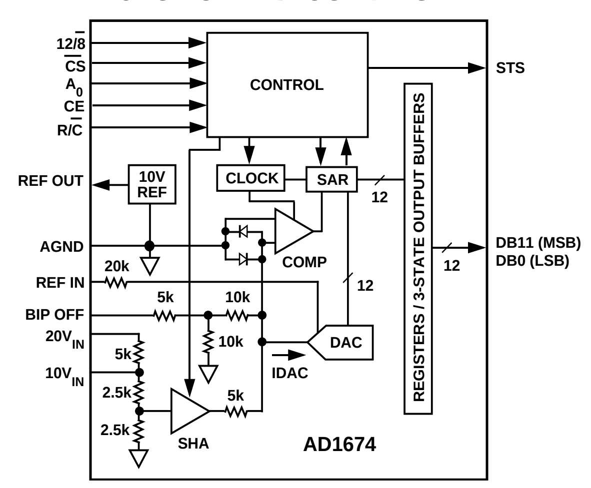
12-Bit 100 kSPS A/D Converter

AD1674*

FEATURES

Complete Monolithic 12-Bit 10 μs Sampling ADC
On-Board Sample-and-Hold Amplifier
Industry Standard Pinout
8- and 16-Bit Microprocessor Interface
AC and DC Specified and Tested
Unipolar and Bipolar Inputs
±5 V, ±10 V, 0 V–10 V, 0 V–20 V Input Ranges
Commercial, Industrial and Military Temperature Range Grades
MIL-STD-883 and SMD Compliant Versions Available

FUNCTIONAL BLOCK DIAGRAM



PRODUCT DESCRIPTION

The AD1674 is a complete, multipurpose, 12-bit analog-to-digital converter, consisting of a user-transparent onboard sample-and-hold amplifier (SHA), 10 volt reference, clock and three-state output buffers for microprocessor interface.

The AD1674 is pin compatible with the industry standard AD574A and AD674A, but includes a sampling function while delivering a faster conversion rate. The on-chip SHA has a wide input bandwidth supporting 12-bit accuracy over the full Nyquist bandwidth of the converter.

The AD1674 is fully specified for ac parameters (such as S/(N+D) ratio, THD, and IMD) and dc parameters (offset, full-scale error, etc.). With both ac and dc specifications, the AD1674 is ideal for use in signal processing and traditional dc measurement applications.

The AD1674 design is implemented using Analog Devices' BiMOS II process allowing high performance bipolar analog circuitry to be combined on the same die with digital CMOS logic.

Five different temperature grades are available. The AD1674J and K grades are specified for operation over the 0°C to +70°C temperature range. The A and B grades are specified from –40°C to +85°C; the AD1674T grade is specified from –55°C to +125°C. The J and K grades are available in both 28-lead plastic DIP and SOIC. The A and B grade devices are available in 28-lead hermetically sealed ceramic DIP and 28-lead SOIC. The T grade is available in 28-lead hermetically sealed ceramic DIP.

***Protected by U. S. Patent Nos. 4,962,325; 4,250,445; 4,808,908; RE30586**.

PRODUCT HIGHLIGHTS

1. Industry Standard Pinout: The AD1674 utilizes the pinout established by the industry standard AD574A and AD674A.
2. Integrated SHA: The AD1674 has an integrated SHA which supports the full Nyquist bandwidth of the converter. The SHA function is transparent to the user; no wait-states are needed for SHA acquisition.
3. DC and AC Specified: In addition to traditional dc specifications, the AD1674 is also fully specified for frequency domain ac parameters such as total harmonic distortion, signal-to-noise ratio and input bandwidth. These parameters can be tested and guaranteed as a result of the onboard SHA.
4. Analog Operation: The precision, laser-trimmed scaling and bipolar offset resistors provide four calibrated ranges: 0 V to +10 V and 0 V to +20 V unipolar, –5 V to +5 V and –10 V to +10 V bipolar. The AD1674 operates on +5 V and ±12 V or ±15 V power supplies.
5. Flexible Digital Interface: On-chip multiple-mode three-state output buffers and interface logic allow direct connection to most microprocessors.

REV. C

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DC SPECIFICATIONS

(T_{MIN} to T_{MAX}, V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5% unless otherwise noted)

	AD1674J			AD1674K			
Parameter	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Unit**
RESOLUTION	12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2	LSB
DIFFERENTIAL NONLINEARITY (DNL)							
(No Missing Codes)	12			12			Bits
UNIPOLAR OFFSET[1] @ +25°C			±3			±2	LSB
BIPOLAR OFFSET[1] @ +25°C			±6			±4	LSB
FULL-SCALE ERROR[1, 2] @ +25°C							
(with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.25	% of FSR
TEMPERATURE RANGE	0		+70	0		+70	°C
TEMPERATURE DRIFT[3]							
Unipolar Offset[2]			±2			±1	LSB
Bipolar Offset[2]			±2			±1	LSB
Full-Scale Error[2]			±6			±3	LSB
POWER SUPPLY REJECTION							
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1	LSB
ANALOG INPUT							
Input Ranges							
Bipolar	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	Volts
	0		+20	0		+20	Volts
Input Impedance							
10 Volt Span	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	kΩ
POWER SUPPLIES							
Operating Voltages							
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–16.5		–11.4	–16.5		–11.4	Volts
Operating Current							
I_{LOGIC}		5	8		5	8	mA
I_{CC}		10	14		10	14	mA
I_{EE}		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4]			2.0			2.0	mA
(External Load Should Not Change During Conversion							

NOTES

[1]Adjustable to zero.

[2]Includes internal voltage reference error.

[3]Maximum change from 25°C value to the value at T_{MIN} or T_{MAX}.

[4]Reference should be buffered for ±12 V operation.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

Parameter	AD1674A Min	AD1674A Typ	AD1674A Max	AD1674B Min	AD1674B Typ	AD1674B Max	AD1674T Min	AD1674T Typ	AD1674T Max	Unit
RESOLUTION	12			12			12			Bits
INTEGRAL NONLINEARITY (INL)			±1			±1/2			±1/2	LSB
			±1			±1/2			±1	LSB
DIFFERENTIAL NONLINEARITY (DNL)										
(No Missing Codes)	12			12			12			Bits
UNIPOLAR OFFSET[1] @ +25°C			±2			±2			±2	LSB
BIPOLAR OFFSET[1] @ +25°C			±6			±3			±3	LSB
FULL-SCALE ERROR[1, 2] @ +25°C										
(with Fixed 50 Ω Resistor from REF OUT to REF IN)		0.1	0.25		0.1	0.125		0.1	0.125	% of FSR
TEMPERATURE RANGE	–40		+85	–40		+85	–55		+125	°C
TEMPERATURE DRIFT[3]										
Unipolar Offset[2]			±2			±1			±1	LSB
Bipolar Offset[2]			±2			±1			±2	LSB
Full-Scale Error[2]			±8			±5			±7	LSB
POWER SUPPLY REJECTION										
V_{CC} = 15 V ± 1.5 V or 12 V ± 0.6 V			±2			±1			±1	LSB
V_{LOGIC} = 5 V ± 0.5 V			±1/2			±1/2			±1/2	LSB
V_{EE} = –15 V ± 1.5 V or –12 V ± 0.6 V			±2			±1			±1	LSB
ANALOG INPUT										
Input Ranges										
Bipolar	–5		+5	–5		+5	–5		+5	Volts
	–10		+10	–10		+10	–10		+10	Volts
Unipolar	0		+10	0		+10	0		+10	Volts
	0		+20	0		+20		0	+20	Volts
Input Impedance										
10 Volt Span	3	5	7	3	5	7	3	5	7	kΩ
20 Volt Span	6	10	14	6	10	14	6	10	14	kΩ
POWER SUPPLIES										
Operating Voltages										
V_{LOGIC}	+4.5		+5.5	+4.5		+5.5	+4.5		+5.5	Volts
V_{CC}	+11.4		+16.5	+11.4		+16.5	+11.4		+16.5	Volts
V_{EE}	–16.5		–11.4	–16.5		–11.4	–16.5		–11.4	Volts
Operating Current										
I_{LOGIC}		5	8		5	8		5	8	mA
I_{CC}		10	14		10	14		10	14	mA
I_{EE}		14	18		14	18		14	18	mA
POWER DISSIPATION		385	575		385	575		385	575	mW
INTERNAL REFERENCE VOLTAGE	9.9	10.0	10.1	9.9	10.0	10.1	9.9	10.0	10.1	Volts
Output Current (Available for External Loads)[4]			2.0			2.0			2.0	mA
(External Load Should Not Change During Conversion										

AD1674–SPECIFICATIONS

AC SPECIFICATIONS

(T_{MIN} to T_{MAX}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ±10% or –12 V ± 5%, f_{SAMPLE} = 100 kSPS, f_{IN} = 10 kHz, stand-alone mode unless otherwise noted)[1]

Parameter	AD1674J/A			AD1674K/B/T			Units
	Min	Typ	Max	Min	Typ	Max	
Signal to Noise and Distortion (S/N+D) Ratio[2, 3]	69	70		70	71		dB
Total Harmonic Distortion (THD)[4]		–90	–82		–90	–82	dB
			0.008			0.008	%
Peak Spurious or Peak Harmonic Component		–92	–82		–92	–82	dB
Full Power Bandwidth		1		1			MHz
Full Linear Bandwidth		500		500			kHz
Intermodulation Distortion (IMD)[5]							
Second Order Products		–90	–80		–90	–80	dB
Third Order Products		–90	–80		–90	–80	dB
SHA (Specifications are Included in Overall Timing Specifications)							
Aperture Delay		50			50		ns
Aperture Jitter		250			250		ps
Acquisition Time		1			1		µs

DIGITAL SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX}, with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ± 10%, V_{EE} = –15 V ± 10% or –12 V ± 5%)

Parameter		Test Conditions	Min	Max	Units
LOGIC INPUTS					
V_{IH}	High Level Input Voltage		+2.0	V_{LOGIC} +0.5 V	V
V_{IL}	Low Level Input Voltage		–0.5	+0.8	V
I_{IH}	High Level Input Current (V_{IN} = 5 V)	$V_{IN} = V_{LOGIC}$	–10	+10	µA
I_{IL}	Low Level Input Current (V_{IN} = 0 V)	V_{IN} = 0 V	–10	+10	µA
C_{IN}	Input Capacitance			10	pF
LOGIC OUTPUTS					
V_{OH}	High Level Output Voltage	I_{OH} = 0.5 mA	+2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 1.6 mA		+0.4	V
I_{OZ}	High-Z Leakage Current	V_{IN} = 0 to V_{LOGIC}	–10	+10	µA
C_{OZ}	High-Z Output Capacitance			10	pF

NOTES

[1] f_{IN} amplitude = –0.5 dB (9.44 V p-p) 10 V bipolar mode unless otherwise noted. All measurements referred to –0 dB (9.997 V p-p) input signal unless otherwise noted.

[2] Specified at worst case temperatures and supplies after one minute warm-up.

[3] See Figures 12 and 13 for other input frequencies and amplitudes.

[4] See Figure 11.

[5] fa = 9.08 kHz, fb = 9.58 kHz with f_{SAMPLE} = 100 kHz. See *Definition of Specifications* section and Figure 15.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

SWITCHING SPECIFICATIONS

(for all grades T_{MIN} to T_{MAX} with V_{CC} = +15 V ± 10% or +12 V ± 5%, V_{LOGIC} = +5 V ±10%, V_{EE} = –15 V ± 10% or –12 V ± 5%; V_{IL} = 0.4 V, V_{IH} = 2.4 V unless otherwise noted)

CONVERTER START TIMING (Figure 1)

Parameter	Symbol	J, K, A, B, Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Conversion Time								
8-Bit Cycle	t_C		7	8		7	8	µs
12-Bit Cycle	t_C		9	10		9	10	µs
STS Delay from CE	t_{DSC}			200			225	ns
CE Pulse Width	t_{HEC}	50			50			ns
$\overline{CS}$ to CE Setup	t_{SSC}	50			50			ns
$\overline{CS}$ Low During CE High	t_{HSC}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRC}	50			50			ns
R/$\overline{C}$ Low During CE High	t_{HRC}	50			50			ns
A_0 to CE Setup	t_{SAC}	0			0			ns
A_0 Valid During CE High	t_{HAC}	50			50			ns

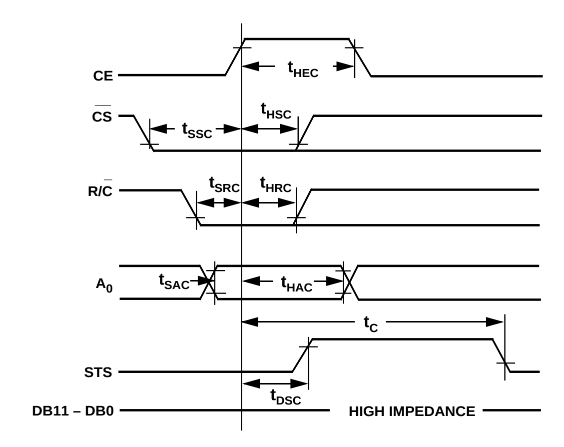


Figure 1. Converter Start Timing

READ TIMING—FULL CONTROL MODE (Figure 2)

Parameter	Symbol	J, K, A, B, Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Access Time	t_{DD}[1]		75	150		75	150	ns
Data Valid After CE Low	t_{HD}	25[2]			25[2]			ns
		20[3]			15[4]			ns
Output Float Delay	t_{HL}[5]			150			150	ns
$\overline{CS}$ to CE Setup	t_{SSR}	50			50			ns
R/$\overline{C}$ to CE Setup	t_{SRR}	0			0			ns
A_0 to CE Setup	t_{SAR}	50			50			ns
$\overline{CS}$ Valid After CE Low	t_{HSR}	0			0			ns
R/$\overline{C}$ High After CE Low	t_{HRR}	0			0			ns
A_0 Valid After CE Low	t_{HAR}	50			50			ns

NOTES

[1] t_{DD} is measured with the load circuit of Figure 3 and is defined as the time required for an output to cross 0.4 V or 2.4 V.

[2] 0°C to T_{MAX}.

[3] At –40°C.

[4] At –55°C.

[5] t_{HL} is defined as the time required for the data lines to change 0.5 V when loaded with the circuit of Figure 3.

All min and max specifications are guaranteed.

Specifications subject to change without notice.

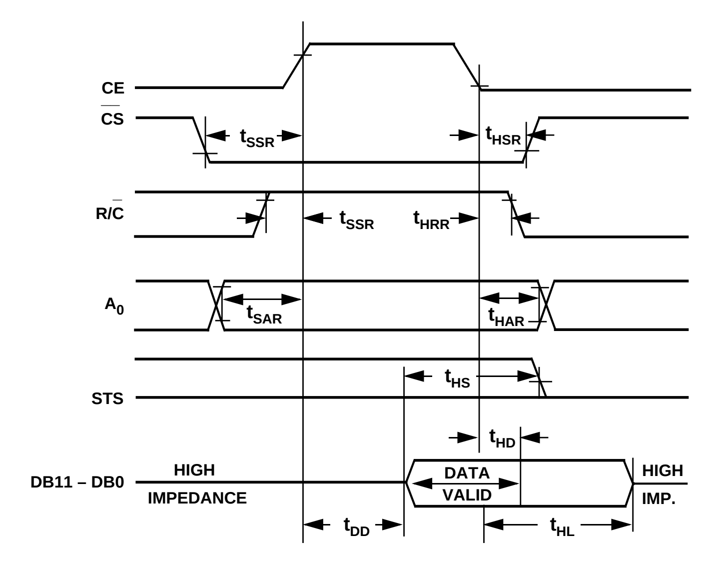


Figure 2. Read Timing

Test	V_{CP}	C_{OUT}
Access Time High Z to Logic Low	5 V	100 pF
Float Time Logic High to High Z	0 V	10 pF
Access Time High Z to Logic High	0 V	100 pF
Float Time Logic Low to High Z	5 V	10 pF

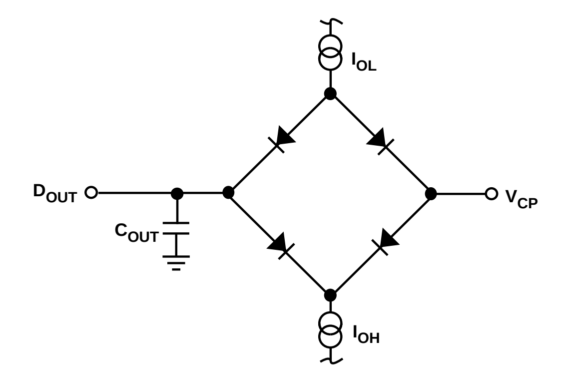


Figure 3. Load Circuit for Bus Timing Specifications

TIMING—STAND-ALONE MODE (Figures 4a and 4b)

Parameter	Symbol	J, K, A, B Grades Min	Typ	Max	T Grade Min	Typ	Max	Units
Data Access Time	t_{DDR}			150			150	ns
Low R/$\overline{C}$ Pulse Width	t_{HRL}	50			50			ns
STS Delay from R/$\overline{C}$	t_{DS}			200			225	ns
Data Valid After R/$\overline{C}$ Low	t_{HDR}	25			25			ns
STS Delay After Data Valid	t_{HS}	0.6	0.8	1.2	0.6	0.8	1.2	µs
High R/$\overline{C}$ Pulse Width	t_{HRH}	150			150			ns

NOTE
All min and max specifications are guaranteed.
Specifications subject to change without notice.

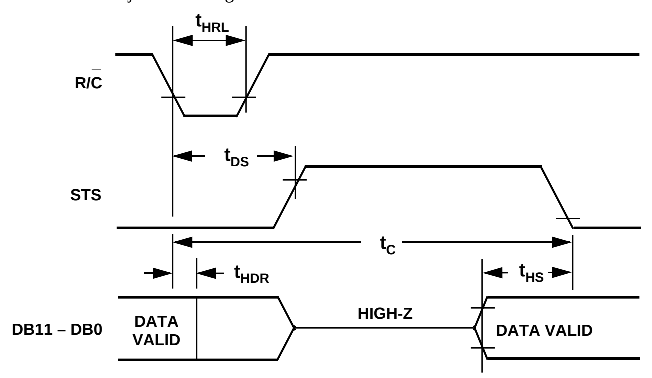


Figure 4a. Stand-Alone Mode Timing Low Pulse for R/$\overline{C}$

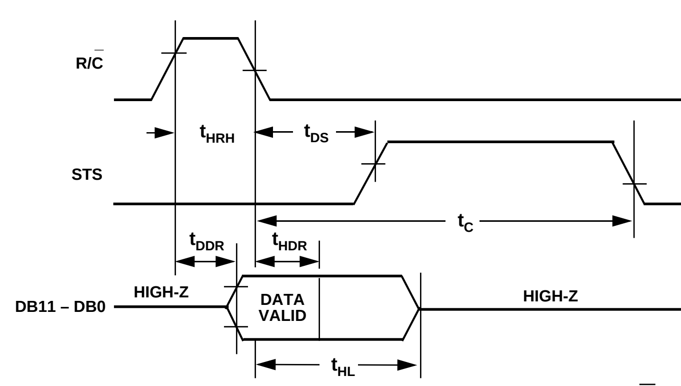


Figure 4b. Stand-Alone Mode Timing High Pulse for R/$\overline{C}$

ABSOLUTE MAXIMUM RATINGS*

V_{CC} to Digital Common . . . . 0 to + 16.5 V
V_{EE} to Digital Common . . . . 0 to –16.5 V
V_{LOGIC} to Digital Common . . . . 0 V to +7 V
Analog Common to Digital Common . . . . ±1 V
Digital Inputs to Digital Common . . . –0.5 V to V_{LOGIC} +0.5 V
Analog Inputs to Analog Common . . . . V_{EE} to V_{CC}
20 V_{IN} to Analog Common . . . . V_{EE} to +24 V
REF OUT . . . . Indefinite Short to Common
. . . . Momentary Short to V_{CC}
Junction Temperature . . . . +175°C
Power Dissipation . . . . 825 mW
Lead Temperature, Soldering (10 sec) . . . . +300°C, 10 sec
Storage Temperature . . . . –65°C to +150°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD1674 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ORDERING GUIDE

Model[1]	Temperature Range	INL (T_{MIN} to T_{MAX})	S/(N+D) (T_{MIN} to T_{MAX})	Package Description	Package Option[2]
AD1674JN	0°C to +70°C	±1 LSB	69 dB	Plastic DIP	N-28
AD1674KN	0°C to +70°C	±1/2 LSB	70 dB	Plastic DIP	N-28
AD1674JR	0°C to +70°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674KR	0°C to +70°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AR	–40°C to +85°C	±1 LSB	69 dB	Plastic SOIC	R-28
AD1674BR	–40°C to +85°C	±1/2 LSB	70 dB	Plastic SOIC	R-28
AD1674AD	–40°C to +85°C	±1 LSB	69 dB	Ceramic DIP	D-28
AD1674BD	–40°C to +85°C	±1/2 LSB	70 dB	Ceramic DIP	D-28
AD1674TD	–55°C to +125°C	±1 LSB	70 dB	Ceramic DIP	D-28

NOTES
[1]For details on grade and package offerings screened in accordance with MIL-STD-883, refer to the Analog Devices Military Products Databook or current AD1674/883B data sheet. SMD is also available.
[2]N = Plastic DIP; D = Hermetic Ceramic DIP; R = Plastic SOIC.

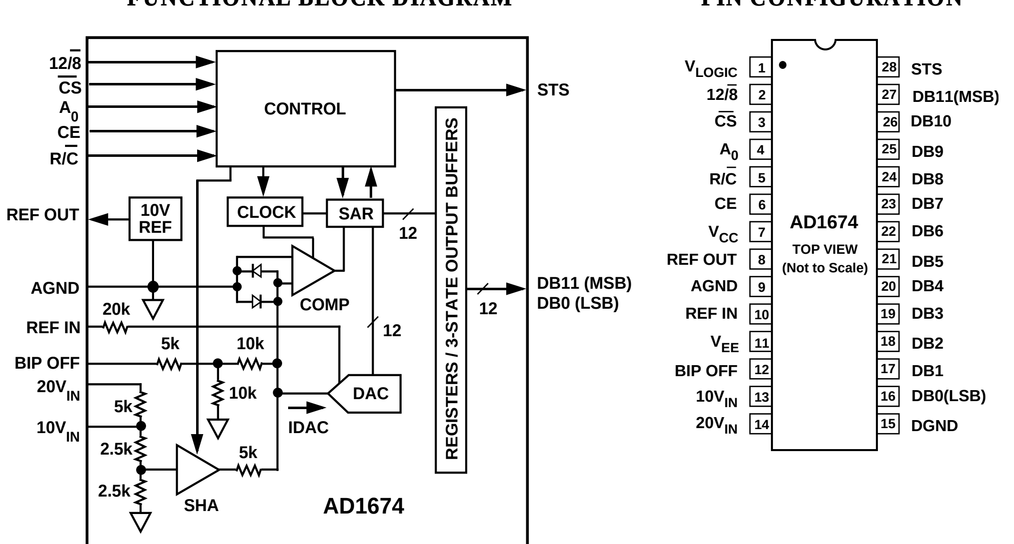
PIN DESCRIPTION

Symbol	Pin No.	Type	Name and Function
AGND	9	P	Analog Ground (Common).
A_0	4	DI	Byte Address/Short Cycle. If a conversion is started with A_0 Active LOW, a full 12-bit conversion cycle is initiated. If A_0 is Active HIGH during a convert start, a shorter 8-bit conversion cycle results. During Read ($R/\overline{C}$ = 1) with $12/\overline{8}$ LOW, A_0 = LOW enables the 8 most significant bits (DB4–DB11), and A_0 = HIGH enables DB3–DB0 and sets DB7–DB4 = 0.
BIP OFF	12	AI	Bipolar Offset. Connect through a 50 Ω resistor to REF OUT for bipolar operation or to Analog Common for unipolar operation.
CE	6	DI	Chip Enable. Chip Enable is Active HIGH and is used to initiate a convert or read operation.
$\overline{CS}$	3	DI	Chip Select. Chip Select is Active LOW.
DB11–DB8	27–24	DO	Data Bits 11 through 8. In the 12-bit format (see $12/\overline{8}$ and A_0 pins), these pins provide the upper 4 bits of data. In the 8-bit format, they provide the upper 4 bits when A_0 is LOW and are disabled when A_0 is HIGH.
DB7–DB4	23–20	DO	Data Bits 7 through 4. In the 12-bit format these pins provide the middle 4 bits of data. In the 8-bit format they provide the middle 4 bits when Ao is LOW and all zeroes when A_0 is HIGH.
DB3–DB0	19–16	DO	Data Bits 3 through 0. In the 12-bit format these pins provide the lower 4 bits of data. In the 8-bit format these pins provide the lower 4 bits of data when A_0 is HIGH, they are disabled when A_0 is LOW.
DGND	15	P	Digital Ground (Common).
REF OUT	8	AO	+10 V Reference Output.
$R/\overline{C}$	5	DI	Read/Convert. In the full control mode $R/\overline{C}$ is Active HIGH for a read operation and Active LOW for a convert operation. In the stand-alone mode, the falling edge of $R/\overline{C}$ initiates a conversion.
REF IN	10	AI	Reference Input is connected through a 50 Ω resistor to +10 V Reference for normal operation.
STS	28	DO	Status is Active HIGH when a conversion is in progress and goes LOW when the conversion is completed.
V_{CC}	7	P	+12 V/+15 V Analog Supply.
V_{EE}	11	P	–12 V/–15 V Analog Supply.
V_{LOGIC}	1	P	+5 V Logic Supply.
10 V_{IN}	13	AI	10 V Span Input, 0 V to +10 V unipolar mode or –5 V to +5 V bipolar mode. When using the AD1674 in the 20 V Span 10 V_{IN} should not be connected.
20 V_{IN}	14	AI	20 V Span Input, 0 V to +20 V unipolar mode or –10 V to +10 V bipolar mode. When using the AD1674 in the 10 V Span 20 V_{IN} should not be connected.
$12/\overline{8}$	2	DI	The $12/\overline{8}$ pin determines whether the digital output data is to be organized as two 8-bit words ($12/\overline{8}$ LOW) or a single 12-bit word ($12/\overline{8}$ HIGH).

TYPE: AI = Analog Input
AO = Analog Output
DI = Digital Input
DO = Digital Output
P = Power

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION



DEFINITION OF SPECIFICATIONS

INTEGRAL NONLINEARITY (INL)

The ideal transfer function for an ADC is a straight line drawn between "zero" and "full scale." The point used as "zero" occurs 1/2 LSB before the first code transition. "Full scale" is defined as a level 1 1/2 LSB beyond the last code transition. Integral nonlinearity is the worst-case deviation of a code from the straight line. The deviation of each code is measured from the middle of that code.

DIFFERENTIAL NONLINEARITY (DNL)

A specification which guarantees no missing codes requires that every code combination appear in a monotonic increasing sequence as the analog input level is increased. Thus every code must have a finite width. The AD1674 guarantees no missing codes to 12-bit resolution; all 4096 codes are present over the entire operating range.

UNIPOLAR OFFSET

The first transition should occur at a level 1/2 LSB above analog common. Unipolar offset is defined as the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 11.

BIPOLAR OFFSET

In the bipolar mode the major carry transition (0111 1111 1111 to 1000 0000 0000) should occur for an analog value 1/2 LSB below analog common. The bipolar offset error specifies the deviation of the actual transition from that point at 25°C. This offset can be adjusted as shown in Figure 12.

FULL-SCALE ERROR

The last transition (from 1111 1111 1110 to 1111 1111 1111) should occur for an analog value 1 1/2 LSB below the nominal full scale (9.9963 volts for 10 volts full scale). The full-scale error is the deviation of the actual level of the last transition from the ideal level at 25°C. The full-scale error can be adjusted to zero as shown in Figures 11 and 12.

TEMPERATURE DRIFT

The temperature drifts for full-scale error, unipolar offset and bipolar offset specify the maximum change from the initial (25°C) value to the value at T_{MIN} or T_{MAX}.

POWER SUPPLY REJECTION

The effect of power supply error on the performance of the device will be a small change in full scale. The specifications show the maximum full-scale change from the initial value with the supplies at various limits.

FREQUENCY-DOMAIN TESTING

The AD1674 is tested dynamically using a sine wave input and a 2048 point Fast Fourier Transform (FFT) to analyze the resulting output. Coherent sampling is used, wherein the ADC sampling frequency and the analog input frequency are related to each other by a ratio of integers. This ensures that an integral multiple of input cycles is captured, allowing direct FFT processing without windowing or digital filtering which could mask some of the dynamic characteristics of the device. In addition, the frequencies are chosen to he "relatively prime" (no common factors) to maximize the number of different ADC codes that are present in a sample sequence. The result, called Prime Coherent Sampling, is a highly accurate and repeatable measure of the actual frequency-domain response of the converter.

NYQUIST FREQUENCY

An implication of the Nyquist sampling theorem, the "Nyquist Frequency" of a converter is that input frequency which is one-half the sampling frequency of the converter.

SIGNAL-TO-NOISE AND DISTORTION (S/N+D) RATIO

S/(N+D) is the ratio of the rms value of the measured input signal to the rms sum of all other spectral components below the Nyquist frequency, including harmonics but excluding dc. The value for S/(N+D) is expressed in decibels.

TOTAL HARMONIC DISTORTION (THD)

THD is the ratio of the rms sum of the first six harmonic components to the rms value of a full-scale input signal and is expressed as a percentage or in decibels. For input signals or harmonics that are above the Nyquist frequency, the aliased component is used.

INTERMODULATION DISTORTION (IMD)

With inputs consisting of sine waves at two frequencies, fa and fb, any device with nonlinearities will create distortion products, of order (m+n), at sum and difference frequencies of mfa ± nfb, where m, n = 0, 1, 2, 3. . . . Intermodulation terms are those for which m or n is not equal to zero. For example, the second order terms are (fa + fb) and (fa – fb) and the third order terms are (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb). The IMD products are expressed as the decibel ratio of the rms sum of the measured input signals to the rms sum of the distortion terms. The two signals are of equal amplitude and the peak value of their sums is –0.5 dB from full scale. The IMD products are normalized to a 0 dB input signal.

FULL-POWER BANDWIDTH

The full-power bandwidth is that input frequency at which the amplitude of the reconstructed fundamental is reduced by 3 dB for a full-scale input.

FULL-LINEAR BANDWIDTH

The full-linear bandwidth is the input frequency at which the slew rate limit of the sample-hold-amplifier (SHA) is reached. At this point, the amplitude of the reconstructed fundamental has degraded by less than –0.1 dB. Beyond this frequency, distortion of the sampled input signal increases significantly.

APERTURE DELAY

Aperture delay is a measure of the SHA's performance and is measured from the falling edge of Read/Convert ($R/\overline{C}$) to when the input signal is held for conversion.

APERTURE JITTER

Aperture jitter is the variation in aperture delay for successive samples and is manifested as noise on the input to the A/D.

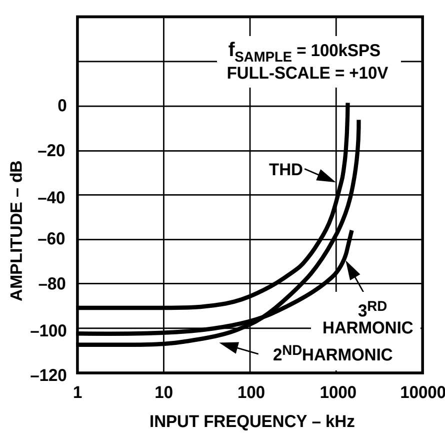


Figure 5. Harmonic Distortion vs. Input Frequency

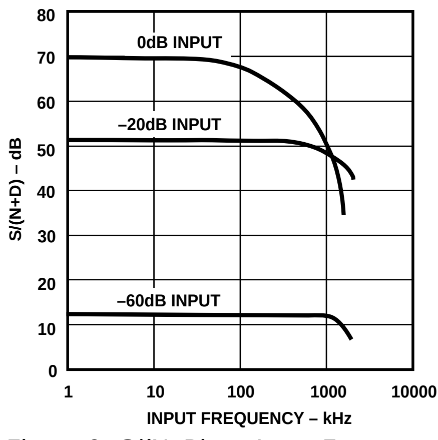


Figure 6. S/(N+D) vs. Input Frequency and Amplitude

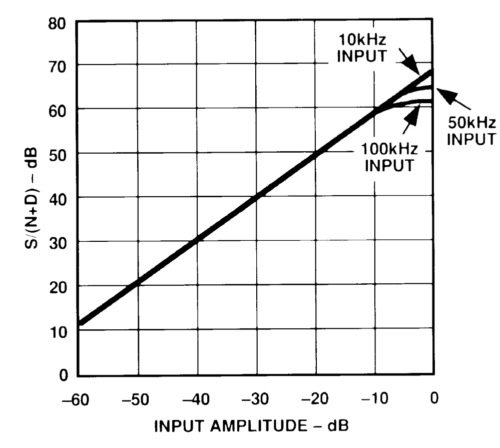


Figure 7. S/(N+D) vs. Input Amplitude

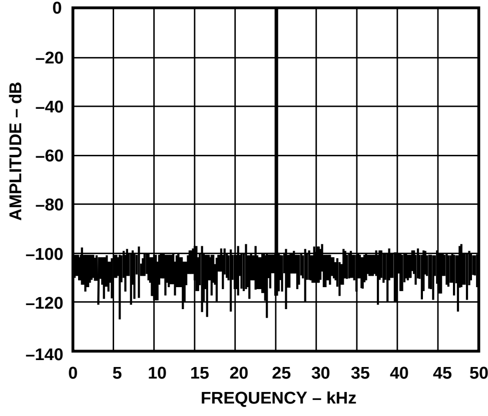


Figure 8. Nonaveraged 2048 Point FFT at 100 kSPS, f_{IN} = 25.049 kHz

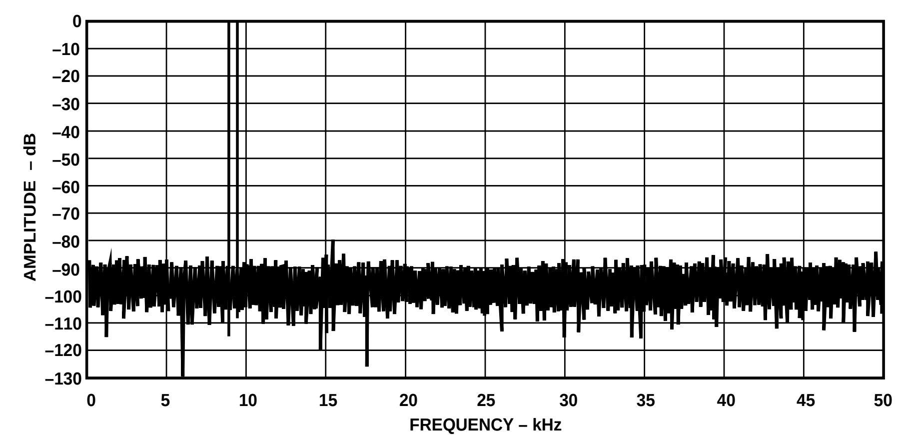


Figure 9. IMD Plot for f_{IN} = 9.08 kHz (fa), 9.58 kHz (fb)

GENERAL CIRCUIT OPERATION

The AD1674 is a complete 12-bit, 10 µs sampling analog-to-digital converter. A block diagram of the AD1674 is shown on page 7.

When the control section is commanded to initiate a conversion (as described later), it places the sample-and-hold amplifier (SHA) in the hold mode, enables the clock, and resets the successive approximation register (SAR). Once a conversion cycle has begun, it cannot be stopped or restarted and data is not available from the output buffers. The SAR, timed by the internal clock, will sequence through the conversion cycle and return an end-of-convert flag to the control section when the conversion has been completed. The control section will then disable the clock, switch the SHA to sample mode, and delay the STS LOW going edge to allow for acquisition to 12-bit accuracy. The control section will allow data read functions by external command anytime during the SHA acquisition interval.

During the conversion cycle, the internal 12-bit, 1 mA full-scale current output DAC is sequenced by the SAR from the most significant bit (MSB) to the least significant bit (LSB) to provide an output that accurately balances the current through the 5 kΩ resistor from the input signal voltage held by the SHA. The SHA's input scaling resistors divide the input voltage by 2 for the 10 V input span and by 4 V for the 20 V input span, maintaining a 1 mA full-scale output current through the 5 kΩ resistor for both ranges. The comparator determines whether the addition of each successively weighted bit current causes the DAC current sum to be greater than or less than the input current. If the sum is less, the bit is left on; if more, the bit is turned off. After testing all the bits, the SAR contains a 12-bit binary code which accurately represents the input signal to within ±1/2 LSB.

CONTROL LOGIC

The AD1674 may be operated in one of two modes, the full-control mode and the stand-alone mode. The full-control mode utilizes all the AD1674 control signals and is useful in systems that address decode multiple devices on a single data bus. The stand-alone mode is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Table I is a truth table for the AD1674, and Figure 10 illustrates the internal logic circuitry.

Table I. AD1674A Truth Table

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_0	Operation
0	X	X	X	X	None
X	1	X	X	X	None
1	0	0	X	0	Initiate 12-Bit Conversion
1	0	0	X	1	Initiate 8-Bit Conversion
1	0	1	1	X	Enable 12-Bit Parallel Output
1	0	1	0	0	Enable 8 Most Significant Bits
1	0	1	0	1	Enable 4 LSBs +4 Trailing Zeroes

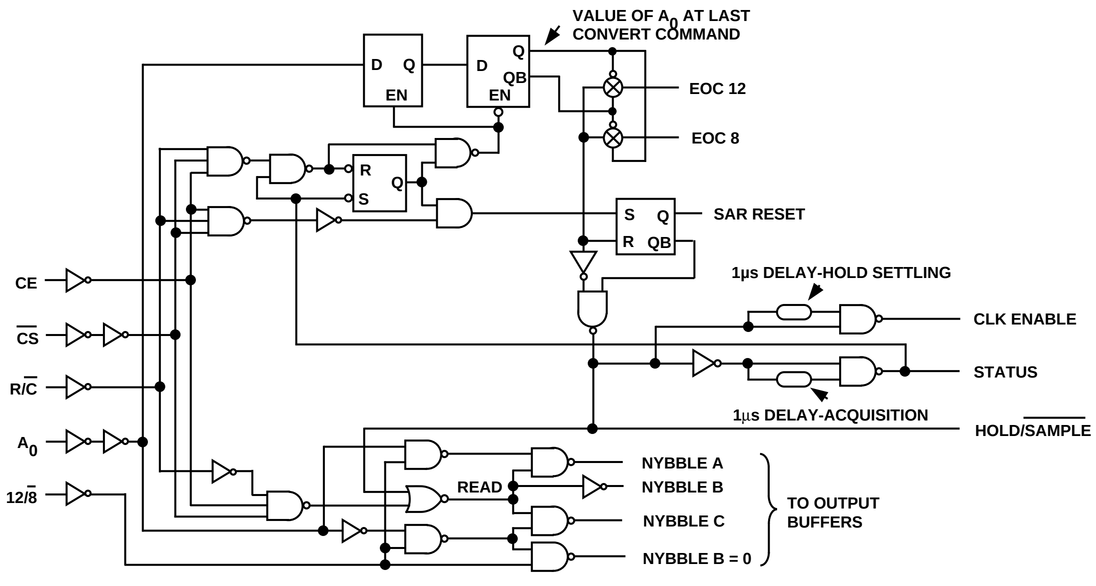


Figure 10. Equivalent Internal Logic Circuitry

FULL-CONTROL MODE

Chip Enable (CE), Chip Select ($\overline{CS}$) and Read/ Convert (R/$\overline{C}$) are used to control Convert or Read modes of operation. Either CE or $\overline{CS}$ may be used to initiate a conversion. The state of R/$\overline{C}$ when CE and $\overline{CS}$ are both asserted determines whether a data Read (R/$\overline{C}$ = 1) or a Convert (R/$\overline{C}$ = 0) is in progress. R/$\overline{C}$ should be LOW before both CE and $\overline{CS}$ are asserted; if R/$\overline{C}$ is HIGH, a Read operation will momentarily occur, possibly resulting in system bus contention.

STAND-ALONE MODE

The AD1674 can be used in a "stand-alone" mode, which is useful in systems with dedicated input ports available and thus not requiring full bus interface capability. Stand-alone mode applications are generally able to issue conversion start commands more precisely than full-control mode. This improves ac performance by reducing the amount of control-induced aperture jitter.

In stand-alone mode, the control interface for the AD1674 and AD674A are identical. CE and 12/$\overline{8}$ are wired HIGH, $\overline{CS}$ and A_0 are wired LOW, and conversion is controlled by R/$\overline{C}$. The three-state buffers are enabled when R/$\overline{C}$ is HIGH and a conversion starts when R/$\overline{C}$ goes LOW. This gives rise to two possible control signals—a high pulse or a low pulse. Operation with a low pulse is shown in Figure 4a. In this case, the outputs are forced into the high impedance state in response to the falling edge of R/$\overline{C}$ and return to valid logic levels after the conversion cycle is completed. The STS line goes HIGH 200 ns after R/$\overline{C}$ goes LOW and returns low 1 µs after data is valid.

If conversion is initiated by a high pulse as shown in Figure 4b, the data lines are enabled during the time when R/$\overline{C}$ is HIGH. The falling edge of R/$\overline{C}$ starts the next conversion and the data lines return to three-state (and remain three-state) until the next high pulse of R/$\overline{C}$.

CONVERSION TIMING

Once a conversion is started, the STS line goes HIGH. Convert start commands will be ignored until the conversion cycle is complete. The output data buffers will be enabled a minimum of 0.6 µs prior to STS going LOW. The STS line will return LOW at the end of the conversion cycle.

The register control inputs, A_0 and 12/$\overline{8}$, control conversion length and data format. If a conversion is started with A_0 LOW, a full 12-bit conversion cycle is initiated. If A_0 is HIGH during a convert start, a shorter 8-bit conversion cycle results.

During data read operations, A_0 determines whether the three-state buffers containing the 8 MSBs of the conversion result (A_0 = 0) or the 4 LSBs (A_0 = 1) are enabled. The 12/$\overline{8}$ pin determines whether the output data is to be organized as two 8-bit words (12/$\overline{8}$ tied LOW) or a single 12-bit word (12/$\overline{8}$ tied HIGH). In the 8-bit mode, the byte addressed when A_0 is high contains the 4 LSBs from the conversion followed by four trailing zeroes. This organization allows the data lines to be overlapped for direct interface to 8-bit buses without the need for external three-state buffers.

INPUT CONNECTIONS AND CALIBRATION

The 10 V p-p and 20 V p-p full-scale input ranges of the AD1674 accept the majority of signal voltages without the need for external voltage divider networks which could deteriorate the accuracy of the ADC.

The AD1674 is factory trimmed to minimize offset, linearity, and full-scale errors. In many applications, no calibration trimming will be required and the AD1674 will exhibit the accuracy limits listed in the specification tables.

In some applications, offset and full-scale errors need to be trimmed out completely. The following sections describe the correct procedure for these various situations.

UNIPOLAR RANGE INPUTS

Figure 11 illustrates the external connections for the AD1674 in unipolar-input mode. The first output-code transition (from 0000 0000 0000 to 0000 0000 0001) should nominally occur for an input level of +1/2 LSB (1.22 mV above ground for a 10 V range; 2.44 mV for a 20 V range). To trim unipolar offset to this nominal value, apply a +1/2 LSB signal between Pin 13 and ground (10 V range) or Pin 14 and ground (20 V range) and adjust R1 until the first transition is located. If the offset trim is not required, Pin 12 can be connected directly to Pin 9; the two resistors and trimmer for Pin 12 are then not needed.

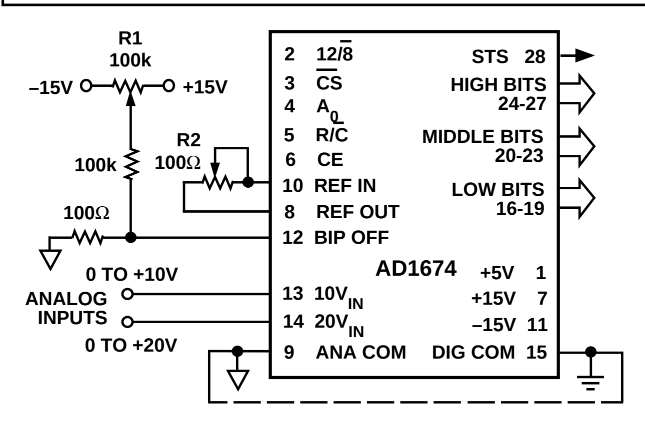


Figure 11. Unipolar Input Connections with Gain and Offset Trims

The full-scale trim is done by applying a signal 1 1/2 LSB below the nominal full scale (9.9963 V for a 10 V range) and adjusting R2 until the last transition is located (1111 1111 1110 to 1111 1111 1111). If full-scale adjustment is not required, R2 should be replaced with a fixed 50 Ω ±1% metal film resistor. If REF OUT is connected directly to REF IN, the additional full-scale error will be approximately 1%.

BIPOLAR RANGE INPUTS

The connections for the bipolar-input mode are shown in Figure 12. Either or both of the trimming potentiometers can be replaced with 50 Ω ± 1% fixed resistors if the specified AD1674 accuracy limits are sufficient for the application. If the pins are shorted together, the additional offset and gain errors will be approximately 1%.

To trim bipolar offset to its nominal value, apply a signal 1/2 LSB below midrange (–1.22 mV for a ±5 V range) and adjust R1 until the major carry transition is located (0111 1111 1111 to 1000 0000 0000). To trim the full-scale error, apply a signal 1 1/2 LSB below full scale (+4.9963 V for a ±5 V range) and adjust R2 to give the last positive transition (1111 1111 1110 to 1111 1111 1111). These trims are interactive so several iterations may be necessary for convergence.

A single-pass calibration can be done by substituting a negative full-scale trim for the bipolar offset trim (error at midscale), using the same circuit. First, apply a signal 1/2 LSB above minus full scale (–4.9988 V for a ±5 V range) and adjust R1 until the minus full-scale transition is located (0000 0000 0001 to 0000 0000 0000). Then perform the gain error trim as outlined above.

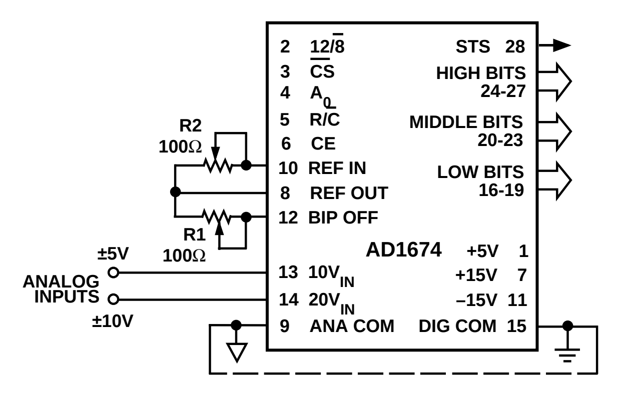


Figure 12. Bipolar Input Connections with Gain and Offset Trims

REFERENCE DECOUPLING

It is recommended that a 10 µF tantalum capacitor be connected between REF IN (Pin 10) and ground. This has the effect of improving the S/(N+D) ratio through filtering possible broad-band noise contributions from the voltage reference.

BOARD LAYOUT

Designing with high resolution data converters requires careful attention to board layout. Trace impedance is a significant issue. At the 12-bit level, a 5 mA current through a 0.5 Ω trace will develop a voltage drop of 2.5 mV, which is 1 LSB for a 10 V full-scale range. In addition to ground drops, inductive and capacitive coupling need to be considered, especially when high accuracy analog signals share the same board with digital signals. Finally, power supplies should be decoupled in order to filter out ac noise.

The AD1674 has a wide bandwidth sampling front end. This means that the AD1674 will "see" high frequency noise at the input, which nonsampling (or limited-bandwidth sampling) ADCs would ignore. Therefore, it's important to make an effort to eliminate such high frequency noise through decoupling or by using an anti-aliasing filter at the analog input of the AD1674.

Analog and digital signals should not share a common path. Each signal should have an appropriate analog or digital return routed close to it. Using this approach, signal loops enclose a small area, minimizing the inductive coupling of noise. Wide PC tracks, large gauge wire, and ground planes are highly recommended to provide low impedance signal paths. Separate analog and digital ground planes are also desirable, with a single interconnection point to minimize ground loops. Analog signals should be routed as far as possible from digital signals and should cross them (if necessary) only at right angles.

The AD1674 incorporates several features to help the user's layout. Analog pins are adjacent to help isolate analog from digital signals. Ground currents have been minimized by careful circuit architecture. Current through AGND is 2.2 mA, with little code-dependent variation. The current through DGND is dominated by the return current for DB11–DB0.

SUPPLY DECOUPLING

The AD1674 power supplies should be well filtered, well regulated, and free from high frequency noise. Switching power supplies are not recommended due to their tendency to generate spikes which can induce noise in the analog system.

Decoupling capacitors should be used in very close layout proximity between all power supply pins and ground. A 10 µF tantalum capacitor in parallel with a 0.1 µF disc ceramic capacitor provides adequate decoupling over a wide range of frequencies.

An effort should be made to minimize the trace length between the capacitor leads and the respective converter power supply and common pins. The circuit layout should attempt to locate the AD1674, associated analog input circuitry, and interconnections as far as possible from logic circuitry. A solid analog ground plane around the AD1674 will isolate large switching ground currents. For these reasons, the use of wire-wrap circuit construction is not recommended; careful printed-circuit construction is preferred.

GROUNDING

If a single AD1674 is used with separate analog and digital ground planes, connect the analog ground plane to AGND and the digital ground plane to DGND keeping lead lengths as short as possible. Then connect AGND and DGND together at the AD1674. If multiple AD1674s are used or the AD1674 shares analog supplies with other components, connect the analog and digital returns together once at the power supplies rather than at each chip. This prevents large ground loops which inductively couple noise and allow digital currents to flow through the analog system.

GENERAL MICROPROCESSOR INTERFACE CONSIDERATIONS

A typical A/D converter interface routine involves several operations. First, a write to the ADC address initiates a conversion. The processor must then wait for the conversion cycle to complete, since most ADCs take longer than one instruction cycle to complete a conversion. Valid data can, of course, only be read after the conversion is complete. The AD1674 provides an output signal (STS) which indicates when a conversion is in progress. This signal can be polled by the processor by reading it through an external three-state buffer (or other input port). The STS signal can also be used to generate an interrupt upon completion of a conversion, if the system timing requirements are critical (bear in mind that the maximum conversion time of the AD1674 is only 10 microseconds) and the processor has other tasks to perform during the ADC conversion cycle. Another possible time-out method is to assume that the ADC will take 10 microseconds to convert, and insert a sufficient number of “no-op” instructions to ensure that 10 microseconds of processor time is consumed.

Once it is established that the conversion is finished, the data can be read. In the case of an ADC of 8-bit resolution (or less), a single data read operation is sufficient. In the case of converters with more data bits than are available on the bus, a choice of data formats is required, and multiple read operations are needed. The AD1674 includes internal logic to permit direct interface to 8-bit or 16-bit data buses, selected by the 12/$\overline{8}$ input. In 16-bit bus applications (12/$\overline{8}$ HIGH) the data lines (DB11 through DB0) may be connected to either the 12 most significant or 12 least significant hits of the data bus. The remaining four bits should be masked in software. The interface to an 8-bit data bus (12/$\overline{8}$ LOW) contains the 8 MSBs (DB11 through DB4). The odd address (A_0 HIGH) contains the 4 LSBs (DB3 through DB0) in the upper half of the byte, followed by four trailing zeroes, thus eliminating bit masking instructions.

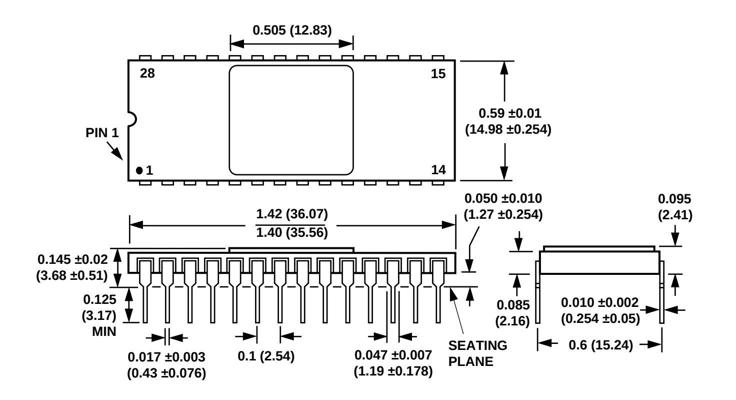
	D7							D0
XXX0 (EVEN ADDR):	DB11 (MSB)	DB10	DB9	DB8	DB7	DB6	DB5	DB4
XXX0 (EVEN ADDR):	DB3	DB2	DB1	DB0 (LSB)	0	0	0	0

AD1674 Data Format for 8-Bit Bus

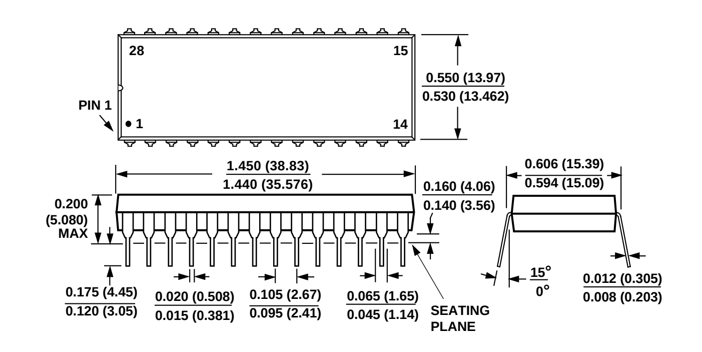
PACKAGE INFORMATION

Dimensions shown in inches and (mm).

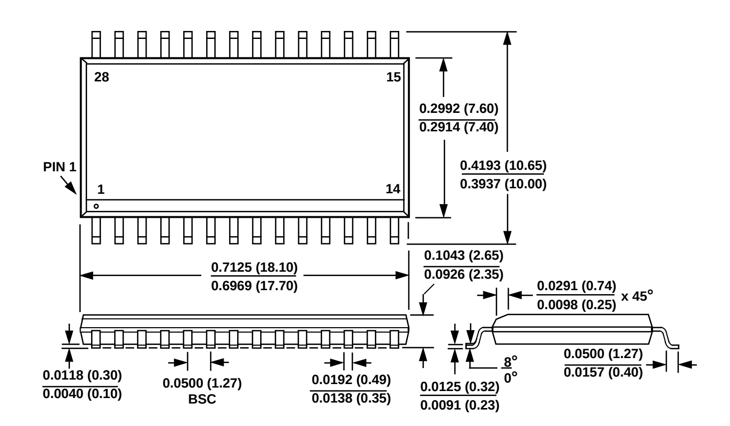
28-Pin Ceramic DIP Package (D-28)



28-Lead Plastic DIP Package (N-28)



28-Lead Wide-Body SO Package (R-28)



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